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PILLSBURY WINTHROP SHAW PITTMAN LLP
P.O. BOX 10500
MCLEAN, VA 22102

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/726,983	BIZJAK, KARL L.	
	Examiner	Art Unit	
	Con P. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-118* is/are pending in the application.

4a) Of the above claim(s) *27-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25,44-46,48-82,100 and 101* is/are rejected.

7)☒ Claim(s) *83-99 and 102-118* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/04/07 has been entered.

Claim Objections

2. Claims 48-49, 83, 90, and 109 are objected to because of the following informalities:

Claim 48 recites the limitation "the plurality of power estimator signals" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 49 recites the limitation "the plurality of power estimator signals" in line 2. There is insufficient antecedent basis for this limitation in the claim (actually, claim 44, line 2, term “power” missing.

Claim 83, line 4, after “to provide an output”, “signal.” needs to be deleted.

Claim 90, line 4, there is a period at the end of line 4.

Claim 109, line 6, there is a period at the end of line 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-5, 8-19, and 100-101** are rejected under 35 U.S.C. 102(b) as being anticipated by Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani").

Regarding **claim 1**, Kitani teaches a compander (see Figs. 1, 4, 5, and respective portions of the specification), comprising:

an input signal (10, Figs. 1, 4, 5);

an input detector (rectifier 13, Figs. 1, 4, 5) for detecting a predetermined condition (i.e., presence) of the input signal (by converting input into DC signal; see col. 6, lines 50-52);

gain calculate logic (including rectifier 13, comparator 15, up/down counter 16; i.e., high, low, second volume 18; Figs. 1, 4, 5) responsive to the input signal (10) and the input detector (i.e., presence of the input signal) for generating a

gain signal (output of 15, up/down counter 16; see col. 1, lines 38-58; col. 6, lines 8-12, 60-67) which creates a gain value (via up/down counter, e.g., counter value is applied to the electronic volume controllers 11 and 18 as a gain control code, col. 1, lines 52-54; also the decoder 18a decodes the counter value output by the up/down counter 16. One or a plurality of switches of the network 18b are selected in response to the output signal of the decoder 18a, so that the constant voltage V_c is divided, see col. 6, lines 32-49; the constant voltage V_c is commonly applied to the electronic volume controllers 69_1 – 69_n, which have different input/output characteristic, gains, with respect to the same counter value applied thereto see also Fig. 21, col. 11, lines 44-59); in other words the gain also including the gain value;

synchronizer logic (including programmable counter 19, first volume 11; Figs. 1, 4, 5, 6) responsive to the input detector (rectifier 13, Figs. 1, 4, 5; e.g., the presence of the input signal) and the gain calculate signal (out put of 15, up/down counter 16) for synchronizing input signal (input V_{in}, Figs. 9A, 13A) and the gain calculate signal to provide an output signal (V_{out} as shown with attack time and recovery time when V_{in} becomes high abruptly, low abruptly, respectively, in Figs. 9B, 9C, 13B; Kitani discloses "if the level of the input signal V_{in} becomes high abruptly" then "During the period, the up/down counter 16 performs the down-count operation on the frequency-divided clock", see col. 7, lines 61 - col. 8, line 1; and "if the level of the input signal V_{in} becomes low abruptly" then "During the above term, the up/down counter 16 performs the up-count operation on the frequency-divided clock", see col. 8, lines 14-21; see also col. 3, lines 29-40; col. 6, lines 18-49; col. 8, lines 1-19, lines 22-32); in other

word synchronizing the input signal and the gain signal when the input detector detecting the presence of the input signal.

Regarding **claim 2**, Kitani teaches wherein the synchronizer logic includes a gain cell (11c, 11b, Figs. 5, 10; col. 8, lines 38-43).

Regarding **claim 3**, Kitani teaches wherein the synchronizer logic further includes a synchronizer block (programmable counter 19 and up/down counter 16; Figs. 4, 5).

Regarding **claim 4**, Kitani teaches wherein the synchronizer block (programmable counter 19 and up/down counter 16; Figs. 4, 5) provides a synchronized gain signal (11c, 11b, Figs. 5, 10; Fig. 33K) and a delayed input signal (Fig. 13G, col. 16, lines 27-46) to the gain cell (col. 16, lines 13-26; lines 47-53), and the gain cell output is the output signal (col. 3, lines 8-13; col. 8, lines 38-43); also see Fig. 32, col. 16, lines 56-59, i.e., the overflow counter (131, Fig. 32) and the clock supply control circuit (133, Fig. 32) enables the up/down counter (16) to perform the up or down count operation only when the signal DATA continues to be high or low for the four cycles or more.

Regarding **claims 5**, Kitani teaches the compander of claim 1 wherein the gain calculate signal is generated only after the predetermined condition (e.g., the presence)

of the input signal occurs (down counting, up counting; col. 7, lines 43-60; see Figs. 9A, 9B, 9C, 13A, 13B;).

Claims 8-9, 11, and 13-15 are also met, i.e., monitoring input logic (col. 3, 44-52), power estimator logic (low pass filter 14, Figs. 4, 5), alternate switching high level, low level; down counting, up counting, peak (col. 7, lines 43-60), average, DC voltage, i.e., RMS, (col. 12, lines 42-67).

Claims 10, 12, and 16-19 are met as above discussion of **Claims 8-9, 11, and 13-15,** reset, i.e., ON/OFF operation of the switch (74a, col. 14, lines 1-9), also please see col. 16, lines 12-55, Figs. 32, 33(A)-33(K).

Claims 100 and 101 are also met since wherein the generated signal value is representative of a time between occurrence of predetermined conditions i.e., the overflow counter (131, Fig. 32) and the clock supply control circuit (133, Fig. 32) enables the up/down counter (16) to perform the up or down count operation only when the signal DATA continues to be high or low for the four cycles or more (see Fig. 32, col. 16, lines 56-59).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Browder U.S. Patent 6,324,229.

Regarding **claim 6,** Kitani teaches the compander of claim 5. However, Kitani does not explicitly disclose wherein the predetermined condition of the input signal further includes a zero crossing. Browder discloses an automatic digital level control applicable to compander (col. 5, lines 1-7) including a zero crossover (320, Fig. 3) couple to gain stage (310) and up/down counter (330; col. 3, lines 41-51) being able to change gain at zero crossover points based on attack and release times (col. 4, lines 46-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate an automatic digital level control of Browder teaching with a compander of Kitani such that the predetermined condition of the input signal further includes a zero crossing as claimed for purpose of avoiding distortion and switching noises, as suggested by Browder in column 4, lines 65-67.

7. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Browder U.S. Patent 6,324,229, and further in view of Thomas U.S. Patent 4,947,133 (cited by Applicant).

Regarding **claim 7,** Kitani in view of Browder teaches the compander of claim 6. However, Kitani in view of Browder does not explicitly disclose wherein the predetermined condition of the input signal further includes a failure to have a zero crossing within a predetermined period. Thomas discloses a failure to have a zero crossing within a predetermined period in col. 6, line 63 – col. 7, line 8 (i.e., exceed delay).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate a predetermine condition of Thomas teaching with the compander of Kitani in view of Browder such that including a failure to have a zero crossing within a predetermined period for purpose of having a control transfer function that may be provided by a digital low-pass filter clocked at zero crossings of the input signal, as suggested by Thomas in column 1, lines 57-59.

8. **Claims 20-23, and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Germer U.S. Patent 4,628,526 (cited by Applicant)

Regarding **claim 20,** Kitani teaches the compander of claim 8. Kitani further teaches wherein the power estimator logic includes initial power estimator logic for determining an initial power estimate (output of LPF 14, Figs. 4, col. 7, lines 43-60), and variable attack and release logic responsive to the initial power estimate (col. 7, lines 61 – col. 8, line 32; Figs. 9A-9C). However, Kitani does not explicitly disclose wherein an initial power estimate for determining a rate of change for the gain calculate signal. Germer discloses matching sound output in which envelope curve detectors (15) and (16) respectively present at the inputs a and b of the comparison circuit (17) are respectively connected to differentiators (19, 20) which responses to changes in envelope curve signals (Figs. 1, 2; col. 6, lines 22-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate differentiators of Germer teaching with compander of Kitani to have an initial power estimate for determining a rate of change for the gain calculate signal as claimed for purpose of having an automatic loudspeaker volume control that is independent of influences of the characteristic of the loudspeaker location, as suggested by Germer in column 2, lines 3-5.

Regarding **claims 21-23,** Kitani as modified teaches a plurality of variable attack and release modules (see Figs 9A-9C), wherein the initial power estimator logic provides at least first and second power estimator signals, and wherein the variable attack and release logic compares the first power estimator signal with the second

power estimator signal (attack time, recovery time become shorter); variable attack and release logic responsive to the initial power estimate (col. 7, lines 61 – col. 8, line 32); .

Regarding **claims 25,** Kitani as modified discloses using plurality of resistors, capacitor for low pass filtering. It would have been obvious to one of ordinary skill in the art to add the initial power estimator which receives as an additional input the output of the variable attack and release logic for purpose of providing both the compressor characteristic and the expander characteristic, as suggested by Kitani in column 3, lines 23-24.

9. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Germer U.S. Patent 4,628,526 (cited by Applicant), and further in view of Orban U.S. Patent 5,444,788.

Regarding **claim 24,** Kitani in view of Germer teaches the compander of claim 20. Kitani further teaches wherein the initial power estimator logic provides at least one power estimator signal to the variable attack and release logic (col. 7, lines 61 – col. 8, line 32). However, Kitani in view of Germer does not explicitly disclose wherein the output of the variable attack and release logic is fed back to provide a second input to the variable attack and release logic.

Orban discloses an audio compressor having a feedback compressor (including VCA 120, rectifier 150, timing circuit 170, and summation means 205, see drawing)

operated as a pilot device coupled between RELEASE TIME control device (210) and the gain of VCA (120; see col. 3, lines 35-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate a feedback compressor of Orban teaching with the compander of Kitani, Germer in combination such that output of the variable attack and release logic is fed back as claimed for purpose of producing a "soft-knee" characteristic, as suggested by Orban in column 4, lines 45-48.

10. **Claims 44-46, 48-49, and 74** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Glaberson U.S. Patent 4,376,916.

Regarding **claims 44,** Kitani teaches a compander having an input comprising at least one power estimator signals (low pass filter 14, Figs. 4, 5), first signal processing stage for processing the at least one power estimator signal (output of LPF 14; col. 7, lines 43-60).

However, Kitani does not explicitly disclose wherein at least one power estimator signal is a plurality of power estimator signals. Glaberson discloses improved signal compression and expansion system in which one power estimator (output of sum 30, Fig. 1) is sum of a plurality of power estimator signals (36, 42, 48; col. 4, lines 39-44; col. 6, lines 46-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate a plurality of power estimator signals of Glaberson teaching with the compander of Kitani so that the at least one power estimate signal is a plurality of power estimator signals for purpose of removal minor ripples not associated with perceptible changes in the information signal, as suggested by Glaberson in column 6, lines 42-45.

Claims 45-46 are also met since Kitani as modified further teaches wherein the processing is demodulating (col. 11, lines 1-10), wherein processing is filtering (output of LPF 14; col. 7, lines 43-60; low pass filtering).

Claim 48 is met since signals are combined at sum 30, Fig. 1.

Regarding **claim 49,** Kitani in view of Glaberson teaches wherein the processing is selecting a preferred one of the plurality of power estimator signals (e.g., 0 dB; see Glaberson, Fig. 4, col. 13, lines 18-31).

Regarding **claim 74,** Kitani teaches the compander of claim 8. However, Kitani does not explicitly disclose:

wherein a first plurality of power estimator signals;

processing stage for generating at least one output signal.

Glaberson discloses improved signal compression and expansion system in which a first plurality of power estimator signals (36, 42, 48; col. 4, lines 39-44; col. 6, lines 46-68);

processing stage for combining at least some of the first plurality of power estimator signals and for generating at least one output signal (output of sum 30, Fig. 1; col. 4, lines 39-44; col. 6, lines 46-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate a plurality of power estimator signals of Glaberson teaching with the compander of Kitani so that to obtain the first plurality of power estimator signals and the processing stage for combining at least some of the first plurality of power estimator signals as claimed for purpose of removal minor ripples not associated with perceptible changes in the information signal, as suggested by Glaberson in column 6, lines 42-45.

11. **Claims 50-73, 75-82** are rejected under 35 U.S.C. 103(a) as being unpatentable over by Armstrong et al. U.S. Patent 5,832,097, cited by Applicant (hereinafter, "Armstrong") in view of Lemson U.S. Patent 5,457,811.

Regarding **claim 50,** Armstrong teaches a device comprising multi-channel synchronous compander (see Figs. 2, 4, 5, 6, and respective portions of the specification; col. 4, lines 31-52) having:

a first input (60, Fig. 2) comprising at least one local voltage signal (high pass output V_{HP}, col. 3, lines 53-67, col. 6, lines 55-67);

a second input (62, Fig. 2) comprising at least one external voltage signal (low pass output V_{LP}, col. 3, lines 53-67, col. 6, lines 55-67);

a first signal processor (summer 68, Fig. 2) for processing the first input (60) and the second input (62) to produce a first output (output of 68, col. 3, lines 53-67, col. 4, lines 29-30).

Armstrong discloses filter outputs in voltage. Armstrong does not explicitly disclose local level signal being local power estimator signal; and external level signal being external estimator signal.

Lemson teaches a dynamic range enhancing system (see Figs. 6, 6a, and respective portions of the specification) in which an AC processor (58, Fig. 6) including a multi-channel spectral analyzer (59, Fig. 6a) being capable of measuring the energy level of filter signals, outputting power estimate levels (i.e. by energy determiners, Fig. 6a) to combiner (60, Fig. 6; col. 26, lines 42-64; col. 29, lines 27-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate dynamic range enhancing system of Lemson teaching with compander of Armstrong to obtain local power estimator signal; and external estimator signal as claimed for purpose of providing dynamic range enhancing system, as suggested by Lemson in column 12, lines 8-9.

Regarding **claim 51,** Armstrong, as modified, further teaches wherein the processing includes combining the first and second inputs (at summer 68, Fig. 4; col. 4, lines 29-30).

Regarding **claim 52,** Armstrong, as modified, further teaches wherein the processing includes selecting one of the first and second inputs (selecting 60 via CRH, Figs. 4, 13; col. 11, lines 31-55).

Regarding **claim 53,** Armstrong, as modified, further teaches wherein the processing includes scaling at least one of the first and second inputs (varying compression ratio of 64 via CRH, Figs. 4, 13; col. 11, lines 31-55).

Regarding **claim 54,** Armstrong in view of Lemson teaches the device of claim 50. Armstrong in view of Lemson, as modified, further teaches wherein second input (Lemson, 61b, Fig. 6) comprises a plurality of external power estimator signals (Lemson, i.e. greater than five inputs, col. 26, lines 29-33; Fig. 6a) and further including a second signal processor (Lemson, AC processor 58, including threshold detector, clock, Fig. 6a; also post-transmission processor, Figs. 9, 11; col. 36, lines 48-58) for processing the plurality of external power estimator signals to produce a single output signal (Lemson, 61b; col. 26, 55-65; col. 29, lines 27-33) to the first signal processor (Armstrong, summer 68, Fig. 2).

Regarding **claims 55-56,** Lemson, as modified, teaches wherein the processing performed by the second signal processor includes combining (for selection, see Fig. 6a), selecting at least some of the plurality of external power estimator signals (i.e. dominant signals, greater than five inputs, col. 26, lines 29-33; see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, lines 27-33; also band 2, control signal demodulator, post-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16).

Regarding **claim 57,** Lemson, as modified, further teaches wherein the processing performed by the second signal processor includes scaling at least one of the plurality of external power estimator signals (weighting, col. 28, lines 5-19; also band 2, control signal demodulator, post-transmission processor, Figs. 9, 11; col. 35, line 66 – col. 36, line 16; col. 36, lines 48-58).

Regarding **claim 58,** Lemson, as modified, teaches wherein the processing performed by the second signal processor includes being capable of demodulating at least one of the plurality of external power estimator signals (col. 5, lines 42-53; also band 2, post transmission processor, Figs. 9, 11; col. 35, line 66 – col. 36, line 16; col. 36, lines 48-58).

Regarding **claim 59,** Lemson, as modified, teaches wherein the processing performed by the second signal processor includes filtering at least one of the plurality of external power estimator signals (BPF, Fig. 6a; 72b, Fig. 9).

Regarding **claim 60,** Armstrong in view of Lemson teaches the device of claim 50. Armstrong in view of Lemson does not explicitly disclose wherein the first input comprises a plurality of local power estimator signals, and further including a third signal processor for processing the plurality of local power estimator signals to produce an exported power estimator signal as claimed.

Nevertheless, it is known in the art to duplicate parts for multiple effects. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

In this regard, Armstrong in view of Lemson, as modified, further teaches the first input comprises a plurality of local power estimator signals, and further including a third signal processor (Lemson, including threshold detector, clock, Fig. 6a; also band 1, control signal modulator, pre-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16) for processing the plurality of local power estimator signals to produce an exported power estimator signal (e.g., different band) as claimed for purpose of increasing capacity of processing signal would have been considered obvious for one of ordinary skill in the art.

Regarding **claim 61,** Lemson, as modified, further teaches wherein the third signal processor comprises a plurality of signal processors, each of which produces an exported power estimator signal signals (see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, 27-33; also band 1, control signal modulator, pre-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16).

Regarding **claims 62-63,** Lemson, as modified, teaches wherein the processing performed by the second signal processor includes combining (for selection, see Fig. 6a), selecting at least some of the plurality of local estimator signals (i.e. dominant signals, greater than five inputs, col. 26, lines 29-33; see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, 27-33; also band 1, control signal modulator, pre-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16).

Regarding **claim 64,** Armstrong, as modified, further teaches wherein the processing performed by the second signal processor includes scaling at least one of the plurality of local power estimator signals (varying compression ratio of 64 via CRH, Figs. 4, 13; col. 11, lines 31-55).

Regarding **claim 65,** Lemson, as modified, teaches wherein the processing performed by the third signal processor includes modulating at least one of the plurality of local power estimator signals (see col. 4, line 64 – col. 5, line 7; also pre transmission processor, Figs. 9, 10; col. 36, lines 3-16).

Regarding **claim 66,** Lemson, as modified, teaches wherein the processing performed by the third signal processor includes filtering at least one of the plurality of local power estimator signals (BPF, Fig. 6a; 72a, Fig. 9).

Regarding **claim 67,** Armstrong in view of Lemson teaches the device of claim 50. Armstrong in view of Lemson does not explicitly disclose further including a second signal for processing the second input signal and a third signal processor for processing the first input signal to produce an exported power estimator signal.

Nevertheless, it is known in the art to duplicate parts for multiple effects. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

In this regard, Armstrong in view of Lemson, as modified, further teaches including a second signal processor (Lemson, AC processor 58, including threshold detector, clock, Fig. 6a; also post-transmission processor, Figs. 9, 11; col. 36, lines 48-58) for processing the second input signal (Armstrong, 62, Fig. 2), and further including a third signal processor (Lemson, including threshold detector, clock, Fig. 6a; also band 1, control signal modulator, pre-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16) for processing the first input signal (Armstrong, 60, Fig. 2) to produce an exported power estimator signal (e.g., different band) as claimed for purpose of increasing capacity of processing signal would have been considered obvious for one of ordinary skill in the art.

Regarding **claim 68,** Armstrong in view of Lemson teaches the compander of claim 67. Armstrong in view of Lemson does not explicitly disclose wherein the second input comprises a plurality of local power estimator signals and the second signal processor processes at least one of the local power estimator signals to produce a single output signal to the first signal processor.

Nevertheless, it is known in the art to duplicate parts for multiple effects. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

In this regard, Armstrong in view of Lemson, as modified, further teaches wherein second input (Lemson, 61b, Fig. 6) comprises a plurality of local power estimator signals (Lemson, i.e. greater than five inputs, col. 26, lines 29-33; Fig. 6a), and further including a third signal processor (Lemson, including threshold detector, clock, Fig. 6a; also band 1, control signal modulator, pre-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16) processes at least one of the local power estimator signals to produce a single output signal (Lemson, 61b; col. 26, 55-65; col. 29, lines 27-33) to the first signal processor (Armstrong, summer 68, Fig. 2) for purpose of increasing capacity of processing signal would have been considered obvious for one of ordinary skill in the art.

Regarding **claim 69,** Armstrong in view of Lemson teaches the device of claim 68. However, Armstrong in view of Lemson does not explicitly disclose wherein the first input comprises a plurality of local power estimator signals, and further including a third signal processor processes the plurality of local power estimator signals to produce an exported power estimator signal.

Nevertheless, it is known in the art to duplicate parts for multiple effects. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

In this regard, Armstrong in view of Lemson, as modified, further teaches the first input comprises a plurality of local power estimator signals, and further including a third

signal processor (Lemson, including threshold detector, clock, Fig. 6a; also band 1, control signal modulator, pre-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16) processes the plurality of local power estimator signals to produce an exported power estimator signal (e.g., different band) as claimed for purpose of increasing capacity of processing signal would have been considered obvious for one of ordinary skill in the art.

Regarding **claim 70** Armstrong in view of Lemson, as modified, further teaches wherein the processing performed by the second signal processor includes demodulating the second input signal (Lemson, col. 5, lines 42-53; post-transmission processor), processing performed by the third signal processor includes modulating the first input signal (Lemson, pre-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16).

Regarding **claim 71,** Armstrong in view of Lemson, as modified, further teaches the processing performed by the second and third signal processor including modulating the first input signal (Lemson, pre-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16; col. 4, line 64 – col. 5, line 7).

Regarding **claims 72-73,** these claims merely reflect the method to the apparatus claim of claims 50 and 54 and are therefore rejected for the same reasons.

Regarding **claim 75,** Armstrong teaches a multi-channel synchronous compander (see Figs. 2, 4, 5, 6, and respective portions of the specification; col. 4, lines 31-52) having:

a first external signal (62, Fig. 2, low pass output V_{LP}, col. 3, lines 53-67, col. 6, lines 55-67);

a first signal processor (summer 68, Fig. 2) for processing the first input (60) and the second input (62) to produce a first output (output of 68, col. 3, lines 53-67, col. 4, lines 29-30) wherein processing includes at least one of a group comprising scaling, combining and selecting the first and second power estimator signals (varying compression ratio of 64 via CRH, Figs. 4, 13; col. 11, lines 31-55).

Armstrong discloses filter outputs in voltage. Armstrong does not explicitly disclose external signal being external estimator signal; and a second external power estimator signal.

Lemson teaches a dynamic range enhancing system (see Figs. 6, 6a, and respective portions of the specification) in which an AC processor (58, Fig. 6) including a multi-channel spectral analyzer (59, Fig. 6a) being capable of measuring the energy level of filter signals, outputting power levels (i.e. by energy determiners, Fig. 6a) to combiner (60, Fig. 6; col. 26, lines 42-64; col. 29, lines 27-41); and a second external power estimator signal (band 2, Fig. 9; col. 35, line 66 – col. 36, line 16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate dynamic range enhancing system of Lemson teaching with compander of Armstrong to obtain local power estimator signal; and

external estimator signal as claimed for purpose of providing dynamic range enhancing system, as suggested by Lemson in column 12, lines 8-9.

Regarding **claim 76,** Lemson, as modified, teaches wherein the processing includes demodulating at least one of the external power estimator signals (col. 5, lines 42-53; also band 2, control signal demodulator, post-transmission processor, Figs. 9, 10, 11; col. 35, line 66 – col. 36, line 16).

Regarding **claim 77,** Armstrong, as modified, teaches wherein the processing includes scaling at least one of the external power estimator signals (varying compression ratio of 64 via CRH, Figs. 4, 13; col. 11, lines 31-55).

Regarding **claim 78,** Lemson, as modified, teaches wherein the processing includes filtering at least one of the external power estimator signals (BPF, Fig. 6a; col. 13, lines 58-64).

Regarding **claim 79,** Lemson teaches the compander of claim 75. Lemson, as modified, teaches further including a second signal processor (Lemson, AC processor 58, including threshold detector, clock, Fig. 6a; also post-transmission processor, Figs. 9, 11; col. 36, lines 48-58) for processing the first output (61b; col. 26, 55-65; col. 29, lines 27-33).

Regarding **claim 80,** Lemson, as modified, teaches wherein the second signal processor modulates the first output (col. 5, lines 42-53; also band 2, post transmission processor, Figs. 9, 11; col. 35, line 66 – col. 36, line 16; col. 36, lines 48-58).

Regarding **claim 81,** Armstrong, as modified, teaches wherein the second signal processor scales the first output (varying compression ratio of 64 via CRH, Figs. 4, 13; col. 11, lines 31-55).

Regarding **claim 82,** Lemson, as modified, teaches wherein the second signal processor filters the first output (BPF, Fig. 6a; col. 13, lines 58-64).

Response to Arguments

12. Applicant's arguments with respect to claim 1 has been considered but are moot in view of the new grounds of rejection. As presented in the Office Action, a presence of the input signal is considered as the predetermined condition.

Allowable Subject Matter

13. Regarding to **claims 83-99, claims 83 and 90** have been amended to incorporate the allowable subject matter, which is indicated by previous Office Action,

would be allowable if rewritten to overcome the objections set forth in this Office action regarding the term "signal." (line 4, claim 83); and the period (line 4, claim 90).

14. Regarding to **claim 109, claim 109** would be allowable if rewritten to overcome the objections set forth in this Office action regarding the period at the end of line 6.

15. The following is a statement of reasons for the indication of allowable subject matter:

16. Regarding new independent **claim 102,** the prior art of record disclosed the compander having power estimator but failed to disclose or render obvious a compander comprising a first input representative of a time between events, a computation engine responsive to the first input and supplying an initial power estimate in accordance with the first input, a second input representative of a signal characteristic associated with the time between events, and combiner logic for combining the initial power estimate with the second input for producing an initial power estimate (same reasons as of claim 83).

17. Regarding new independent **claim 109,** the prior art of record disclosed the compander having filter circuit but failed to disclose or render obvious a compander comprising a first input representative of a time between events, a computation engine responsive to the first input and supplying filter parameters in accordance with the first

input, a second input representative of a signal characteristic associated with the time between events, and a filter responsive to the filter parameters for processing the second input for producing an initial power estimate (same reasons as of claim 90).

18. Claims 103-108 are allowed by virtue of their dependency on claim 102.

19. Claims 110-118 are allowed by virtue of their dependency on claim 109.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Con P. Tran whose telephone number is (571) 272-7532. The examiner can normally be reached on M - F (8:30 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Vivian C. Chin can be reached on (571) 272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cpt CPJ
November 20, 2007

VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600